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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/915,366	07/27/2001	Yasuhito Suzuki	50090-309	6983

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EXAMINER
VU, QUANG D

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 07/18/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/915,366	SUZUKI ET AL.
	Examiner	Art Unit
	Quang D Vu	2811

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-13 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-13 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 4 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 9-13 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

A broad range or limitation together with a narrow range or limitation that falls within the broad range or limitation (in the same claim) is considered indefinite, since the resulting claim does not clearly set forth the metes and bounds of the patent protection desired. Note the explanation given by the Board of Patent Appeals and Interferences in *Ex parte Wu*, 10 USPQ2d 2031, 2033 (Bd. Pat. App. & Inter. 1989), as to where broad language is followed by "such as" and then narrow language. The Board stated that this can render a claim indefinite by raising a question or doubt as to whether the feature introduced by such language is (a) merely exemplary of the remainder of the claim, and therefore not required, or (b) a required feature of the claims. Note also, for example, the decisions of *Ex parte Steigewald*, 131 USPQ 74 (Bd. App. 1961); *Ex parte Hall*, 83 USPQ 38 (Bd. App. 1948); and *Ex parte Hasche*, 86 USPQ 481 (Bd. App. 1949). In the present instance, claim 9 recites the broad recitation each of the plurality of semiconductor packages, and the claim also recites a semiconductor package which is the narrower statement of the range/limitation.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 4,729,010 to Tsuchiya et al.

Regarding claim 1, Tsuchiya et al. teach a semiconductor package comprising:

a die pad (1);

a die mounted on the die pad (6);

a plurality of outer leads (3) electrically connected to electrodes of the die by bonding wires, respectively; and

wherein the outer leads have upper electrical connecting surfaces on the side of the upper surface of the sealing member, and lower electrical connecting surfaces on the side of the lower surface of the sealing member, respectively, and the outer leads have a height from a plane including the lower surface of the sealing member greater than that of the upper surface of the sealing member from the same plane (see figures 1, 3-5)

Tsuchiya et al. do not teach a sealing member sealing therein the die, the bonding wires, parts of the outer leads and a part of the die pad, and having an upper surface on the side of the die and a lower surface on the side of the die pad. Tsuchiya et al. teach the cap member. It would have been obvious to one having ordinary skill in the art at the time the invention was

made to include the sealing member, since the sealing member can be use to seal the semiconductor elements together.

Regarding claim 2, Tsuchiya et al. teach the upper electrical connecting surfaces of the outer leads formed on the side of the upper surface of the cap member lie outside a projection region of the upper surface of the sealing member (see figures 1 and 3). Tsuchiya et al. do not teach the sealing member. It would have been obvious to one having ordinary skill in the art at the time the invention was made to include the sealing member, since the sealing member can be use to seal the semiconductor elements together.

Regarding claim 3, Tsuchiya et al. teach the outer leads are formed on the cap member. Tsuchiya et al. do not teach the sealing member. It would have been obvious to one having ordinary skill in the art at the time the invention was made to include the sealing member, since the sealing member can be use to seal the semiconductor elements together.

Regarding claim 4, Tsuchiya et al. teach the outer leads are formed in an L-shape (see figures 1 and 3).

5. Claims 5-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 4,729,010 to Tsuchiya et al. in view of JP Patent No. 05-183103 to Hiraiwa.

Regarding claim 5, Tsuchiya et al. teach a semiconductor device, comprising:

a printed wiring board; and

a die pad;

a die mounted on the die pad;

the outer leads electrically connected to electrodes of the die by bonding wires, respectively; and

wherein the outer leads have upper electrically connecting surfaces on the side of the upper surface of the sealing member, and lower electrical connecting surfaces on the side of the lower surface of the sealing member, respectively, and the outer leads have a height from a plane including the lower surface of the sealing member greater than that of the upper surface of the sealing member from the same plane.

Tsuchiya et al. do not teach a plurality of semiconductor packages, stacked up on the printed wiring board with outer leads included therein; wherein each of the plurality of semiconductor packages comprises. Hiraiwa teaches a plurality of semiconductor packages, stacked up on the printed wiring board with outer leads included therein; wherein each of the plurality of semiconductor packages comprises. It would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Hiraiwa into the device taught by Tsuchiya et al., since it is a design choice to include the plurality of semiconductor packages.

Tsuchiya et al. do not teach a sealing member sealing therein the die, the bonding wires, parts of the outer leads and a part of the die pad, and having an upper surface on the side of the die and a lower surface on the side of the die pad. Tsuchiya et al. teach the cap member. It would have been obvious to one having ordinary skill in the art at the time the invention was made to include the sealing member, since the sealing member can be use to seal the semiconductor elements together.

Regarding claim 6, Tsuchiya et al. teach the upper electrical connecting surfaces of the outer leads formed on the side of the upper surface of the cap member lie outside a projection surface of the cap member lie outside a projection region of the upper surface of the cap member. Tsuchiya et al. do not teach the upper electrical connecting surfaces of the outer leads formed on the side of the upper surface of the sealing member lie outside a projection surface of the sealing member lie outside a projection region of the upper surface of the sealing member. However, Hiraiwa teaches the sealing member (see figure 1). It would have been obvious to one having ordinary skill in the art at the time the invention was made to include the sealing member, since the sealing member can be use to seal the semiconductor elements together.

Regarding claim 7, Tsuchiya et al. teach the outer leads are formed on the cap member. Tsuchiya et al. do not teach the sealing member. It would have been obvious to one having ordinary skill in the art at the time the invention was made to include the sealing member, since the sealing member can be use to seal the semiconductor elements together.

Regarding claim 8, Tsuchiya et al. teach the outer leads are formed in an L-shape (see figures 1 and 3).

Regarding claim 9, Tsuchiya et al. teach

a semiconductor device comprising:

a printed wiring board, and

a die pad,

a die mounted on the die pad;

the outer leads electrically connected to electrodes of the die by bonding wires, respectively; and

wherein the outer leads have upper electrical connecting surfaces on the side of the upper surface of the sealing member, and lower electrical connecting surfaces on the side of the lower surface of the sealing member, respectively, and the outer leads have a height from a plane including the lower surface of the sealing member greater than that of the upper surface of the sealing member from the same plane.

Tsuchiya et al. do not teach the sealing member sealing therein the die, the bonding wires, parts of the outer leads and a part of the die pad, and having the upper surface o the side of the die and a lower surface on the side of the die pad. Tsuchiya et al. teach the cap member. It would have been obvious to one having ordinary skill in the art at the time the invention was made to include the sealing member, since the sealing member can be use to seal the semiconductor elements together.

Regarding claim 10, Tsuchiya et al. teach the upper electrical connecting surfaces of the outer leads formed on the side of the upper surface of the cap member lie outside a projection region of the upper surface of the sealing member (see figures 1 and 3). Tsuchiya et al. do not teach the sealing member. It would have been obvious to one having ordinary skill in the art at the time the invention was made to include the sealing member, since the sealing member can be use to seal the semiconductor elements together.

Regarding claim 11, Tsuchiya et al. teach the outer leads are formed on the cap member. Tsuchiya et al. do not teach the sealing member. It would have been obvious to one having ordinary skill in the art at the time the invention was made to include the sealing member, since the sealing member can be use to seal the semiconductor elements together.

Regarding claim 12, Tsuchiya et al. teach the outer leads are formed in an L-shape (see figures 1 and 3).

Regarding claim 13, Tsuchiya et al. teach the die pad of the semiconductor package is provided on is exposed surface with a cooling fin.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quang D Vu whose telephone number is 703-305-3826. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 703-308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

QVU
July 15, 2002

Sara Crane
Primary Examiner